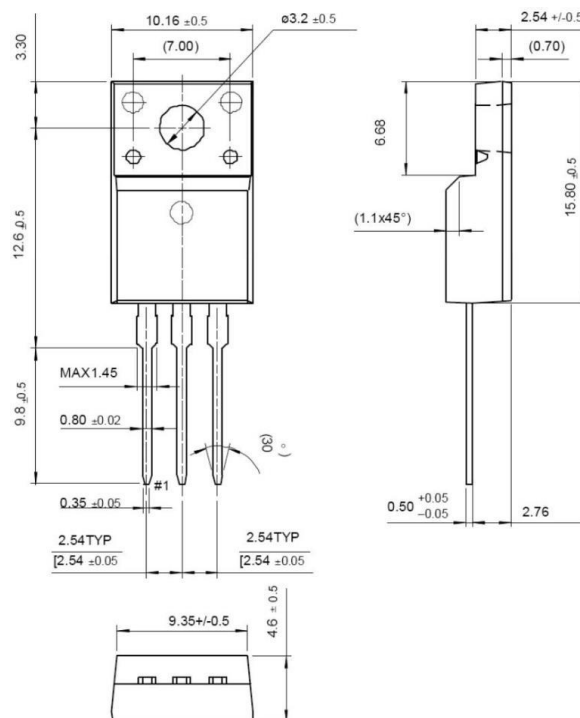
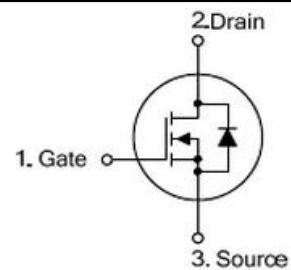
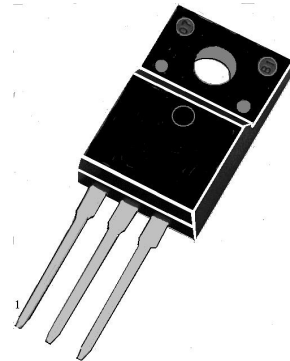


### ◆ Features:

- ✧ Fast switching speed  
开关速度快
- ✧ High input impedance and low level drive  
高输入阻抗和低电平驱动
- ✧ Avalanche energy tested  
雪崩能量测试
- ✧ Improved dv/dt capability, high ruggedness  
提高 dv/dt 能力, 高耐用性

### ◆ Applications

- ✧ High efficiency switch mode power supplies  
高效率开关电源
- ✧ Power factor correction  
功率因数校正
- ✧ Electronic lamp ballast  
电子整流器


**TO-220F**


**◆ Absolute Maximum Ratings (Tc=25°C)**

Symbol	Parameters	Ratings	Unit
V <sub>DSS</sub>	Drain-Source Voltage 漏源电压	<b>600</b>	V
V <sub>GS</sub>	Gate-Source Voltage-Continuous 栅源电压	<b>±30</b>	V
I <sub>D</sub>	Drain Current-Continuous (Note 2) 漏极持续电流	<b>12</b>	A
I <sub>DM</sub>	Drain Current-Single Plused (Note 1) 漏极单次脉冲电流	<b>48</b>	A
P <sub>D</sub>	Power Dissipation (Note 2) 功率损耗	<b>51</b>	W
T <sub>j</sub>	Max.Operating junction temperature 最大结温	<b>150</b>	°C

**◆ Electrical characteristics (Tc=25°C unless otherwise noted)**

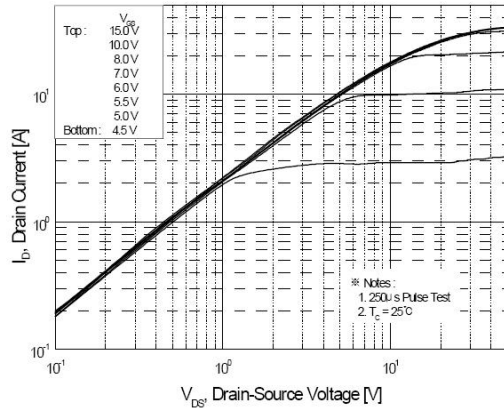
Symbo l	Parameters	Min	Typ	Max	Units	Conditions
<b>Static Characteristics</b>						
B <sub>V</sub> DSS	Drain-Source Breakdown VoltageCurrent (Note 1) 漏极击穿电压	<b>600</b>	--	--	mA	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C
V <sub>GS(th)</sub>	Gate Threshold Voltage 栅极开启电压	<b>2.0</b>	--	<b>4.0</b>	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
R <sub>DS(on)</sub>	Drain-Source On-Resistance 漏源导通电阻	--	<b>0.6</b>	<b>0.85</b>	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =6A
I <sub>GSS</sub>	Gate-Body Leakage Current 栅极漏电流	--	--	<b>±100</b>	nA	V <sub>GS</sub> =±30V, V <sub>DS</sub> =0
I <sub>DSS</sub>	Zero Gate Voltage Drain Current 零栅极电压漏极电流	--	--	<b>1</b>	μA	V <sub>DS</sub> =600V, V <sub>GS</sub> =0
g <sub>fs</sub>	Forward Transconductance 正向跨导	--	<b>3.8</b>	--	S	V <sub>DS</sub> =40V, I <sub>D</sub> =6A

Switching Characteristics						
T <sub>d (on)</sub>	Turn-On Delay Time 开启延迟时间	--	30	70	ns	V <sub>DS</sub> =300V, I <sub>D</sub> =6A, R <sub>G</sub> =25Ω (Note 2)
T <sub>r</sub>	Rise Time 上升时间	--	115	240	ns	
T <sub>d (off)</sub>	Turn-Off Delay Time 关闭延迟时间	--	95	200	ns	
T <sub>f</sub>	Fall Time 下降时间	--	85	180	ns	
Q <sub>g</sub>	Total Gate Charge 栅极总电荷	--	45	54	nC	V <sub>DS</sub> =480V , V <sub>GS</sub> =10V, I <sub>D</sub> =12A (Note 2)
Q <sub>gs</sub>	Gate-Source Charge 栅源极电荷	--	8.5	--	nC	
Q <sub>gd</sub>	Gate-Drain Charge 栅漏极电荷	--	21	--	nC	
Dynamic Characteristics						
C <sub>iss</sub>	Input Capacitance 输入电容	--	1480	1900	pF	V <sub>DS</sub> =25V, V <sub>GS</sub> =0, f=1MHz
C <sub>oss</sub>	Output Capacitance 输出电容	--	200	270	pF	
C <sub>rss</sub>	Reverse Transfer Capacitance 反向传输电容	--	25	35	pF	
I <sub>S</sub>	Continuous Drain-Source Diode Forward Current (Note 2) 二极管导通正向持续电流	--	--	12	A	
V <sub>SD</sub>	Diode Forward On-Voltage 二极管正向导通电压	--	--	1.3	V	I <sub>S</sub> =12A, V <sub>GS</sub> =0
R <sub>th(j-c)</sub>	Thermal Resistance, Junction to Case 结到外壳的热阻	--	--	3.65	℃/W	

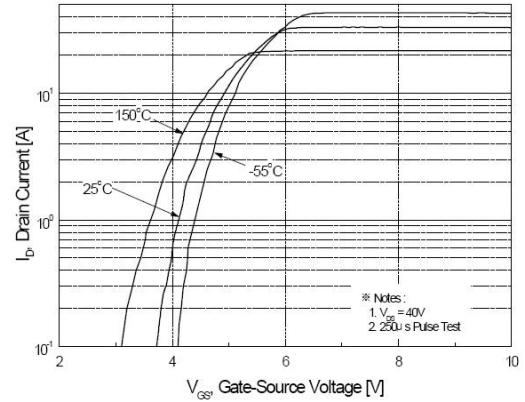
Note 1: Repetitive Rating : Pulse width limited by maximum junction temperature

Note 2: Pulse test:  $PW \leq 300\mu s$ , duty cycle  $\leq 2\%$ .

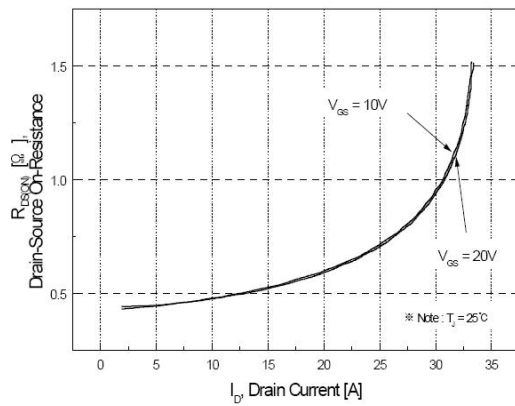
# ◆ Ratings and Characteristic curves



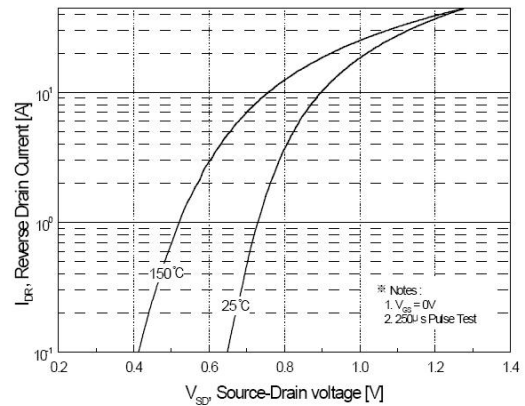
**Figure 1. On-Region Characteristics**



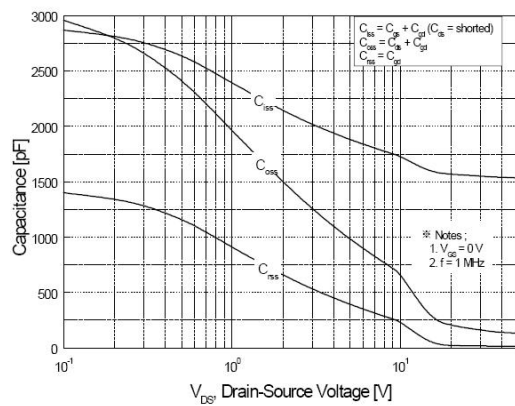
**Figure 2. Transfer Characteristics**



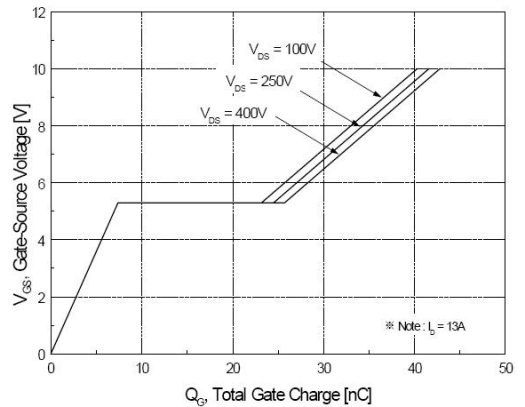
**Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage**



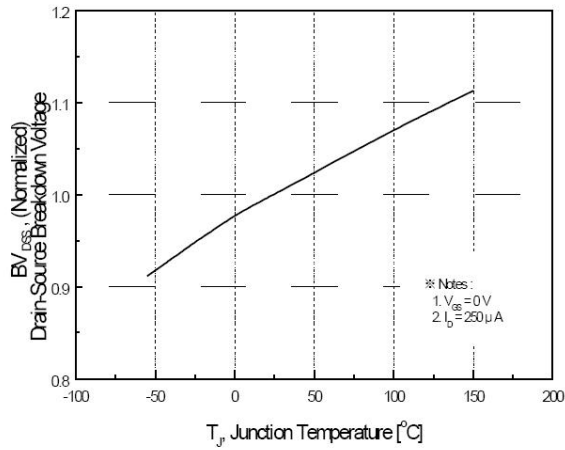
**Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature**



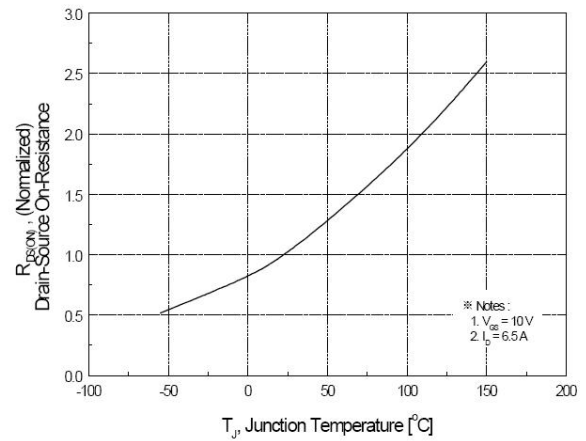
**Figure 5. Capacitance Characteristics**



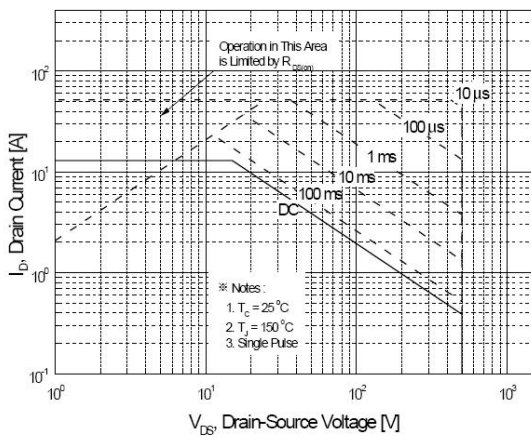
**Figure 6. Gate Charge Characteristics**



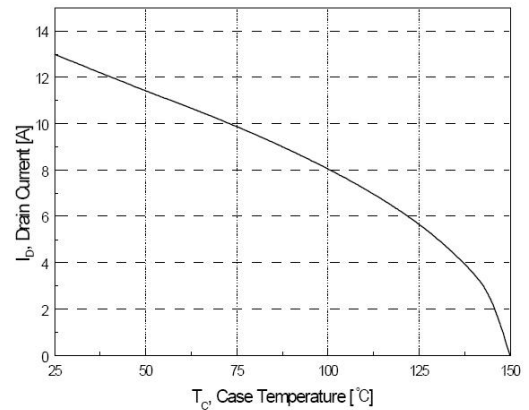
**Figure 7. Breakdown Voltage Variation vs Temperature**



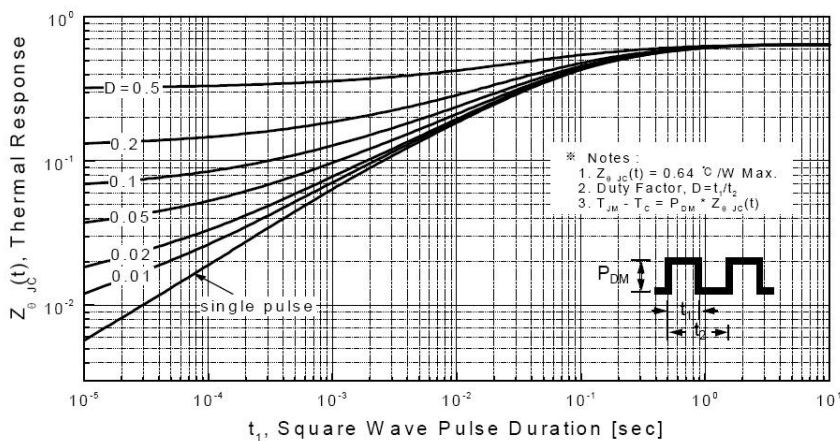
**Figure 8. On-Resistance Variation vs Temperature**



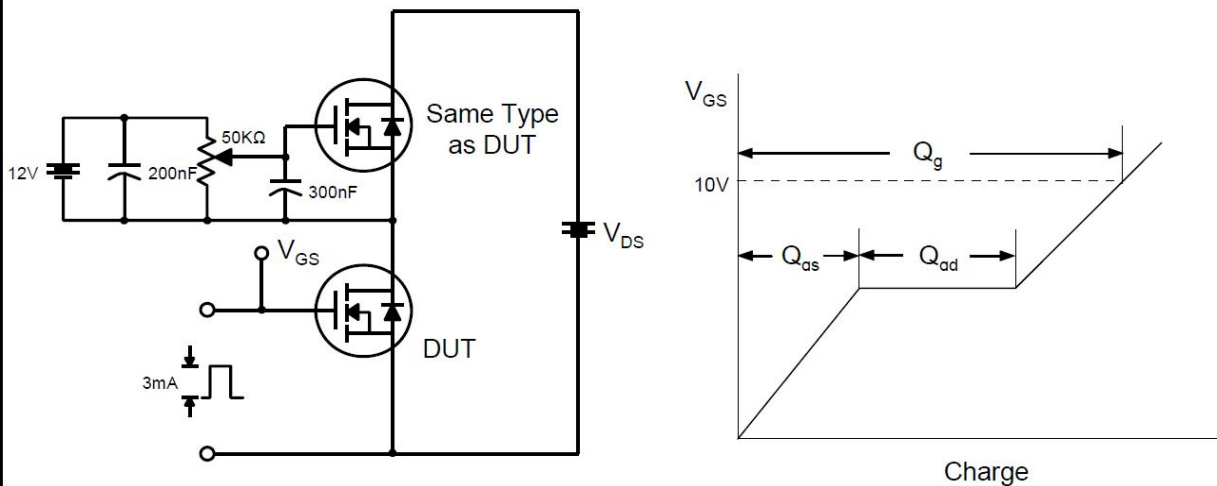
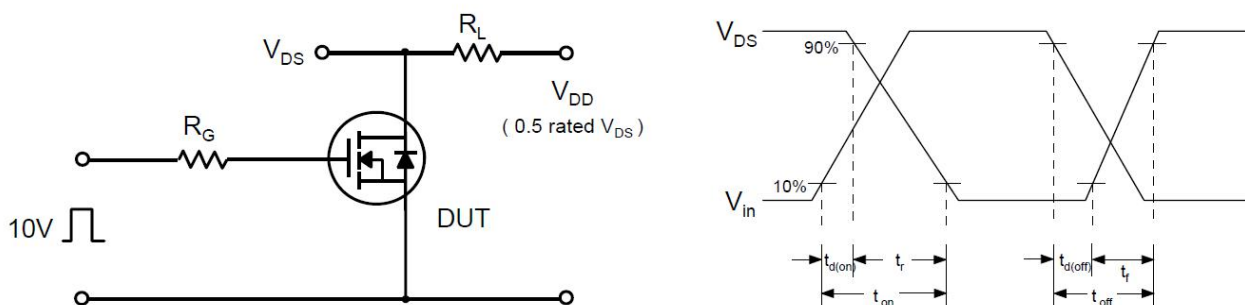
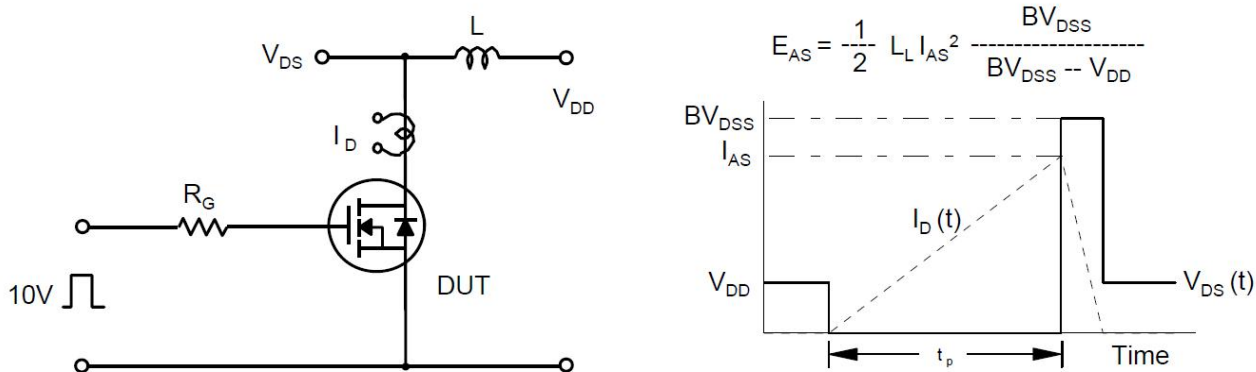
**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs Case Temperature**



**Figure 11. Transient Thermal Response Curve**

**Fig 12. Gate Charge Test Circuit & Waveform**

**Fig 13. Resistive Switching Test Circuit & Waveforms**

**Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms**




**Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms**
